Form PTO-1449 U.S. Department of Commerce Patent and Trademark Office	Docket No. D5116-00002	Serial No. 09/675,427
INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION (Use several sheets if necessary)	Applicant Saxena et al.	
	Filing Date September 29, 2000	Group Art Unit 2812

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
H.D.	AA	5,767,542	6/16/98	Nakamura	57	296	
H.D.	AB	5,773,315	6/30/98	Jarvis	438	14	
H.D.	AC	6,184,048	2/6/01	Ramon	438	14	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
								X
								X

OTHER (Including Author, Title, Date, Pertinent Pages, Etc.)

H.D.	A	International Search Report dated 09 APR 2001
H.D.	B	Khare et al., "Extraction of Defect Characteristics for Yield Estimation Using The Double Bridge Test Structure", IEEE, May 1991, pages 428-432
H.D.	C	Yun et al., "Evaluating the Manufacturability of GaAs/AlGaAs Multiple Quantum Well Avalanche Photodiodes Using Neural Networks, IEEE, Oct 1997, pages 105-112
H.D.	D	Hansen et al., "Effectiveness of Yield-Estimation and Reliability-Prediction Based on Wafer Test-Chip Measurements", IEEE, Jan 1997, pages 142-148

EXAMINER Hoang-Quan Ngo DATE CONSIDERED 3/24/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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H.D.	A	3,751,647	8/7/73	Maeder et al.	235	151.11	
H.D.	B	5,822,258	10/13/98	Casper	365	201	
H.D.	C	5,852,581	12/22/98	Beffa et al	365	201	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER (Including Author, Title, Date, Pertinent Pages, Etc.)

H.D.	D	Khare et al., "Yield Oriented Computer-Aided Defect Diagnosis", IEEE Trans. on Semiconductor Manufacturing, Vol. 8, No. 02, May 1995 (02.05.1995), pages 195-206
H.D.	E	International Search Report dated 08 JUN 2001

EXAMINER Hezron-del Day DATE CONSIDERED 3/24/05

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	Filing Date November 29,2000	Group Art Unit 2812

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
H.D	A	4,835,466	5/30/89	Maly et al.	324	158R	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	NO

OTHER (Including Author, Title, Date, Pertinent Pages, Etc.)

H.D	B	Nurani et al., "In-Line Yield Prediction Methodologies Using Patterned Wafer Inspection Information", IEEE Transactions on Semiconductor Manufacturing, Vol. 11, No. 1, Feb 1998, pp.40-47

EXAMINER Heung-Ku Dang	DATE CONSIDERED 3/24/05

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	09/675,427
Filing Date	September 29, 2000
First Named Inventor	Sharad Saxena
Art Unit	2128
Examiner Name	Morella I Rosales Hanner
Attorney Docket Number	D5116-00002

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
H.D.		Y. CHENG et al., "MOSFET Modeling and BSIM User Guide." Kluwer Academic Publishers, Boston, 1999	✓
H.D.		CONTI et al. "Parametric Yield Formulation of MOS IC's Affected by Mismatch Effect." IEEE Transactions on Computer-Aided Design, Vol. 18, pp. 582-596, May 1999	
H.D.		GUARDIANI et al., "Applying a submicron mismatch model to practical IC design." IEEE Custom Integrated Circuits Conference, San Diego (CA), May 1994	
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H.D.		PINEDA DE GYVEZ et al., "Integrated Circuits Manufacturability: the Art of Process and Design Integration." pp. 158-166, IEEE Press, New York, 1999	
H.D.		FELT et al., "Hierarchical Statistical Characterization of Mixed-Signal Circuits Using Behavioral Modeling." IEEE-ACM International Conference on Computer Aided Design, San Jose (CA), November 1996	
H.D.		MICHAEL et al., "Statistical Modeling for Computer-Aided Design of MOS VLSI Circuits." Kluwer Academic Publishers, Boston, 1993	
H.D.		MICHAEL et al., "Statistical Modeling of Device Mismatch for Analog Integrated Circuits." IEEE Journal of Solid-State Circuits, Vol. 27, No. 2, February 1992	
H.D.		"pdPCA User's Manual." Version 7, PDF Solutions, Inc., San Jose, 1998	

Examiner Signature	Hanner	Date Considered	3/24/05

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	09/675,427
Filing Date	September 29, 2000
First Named Inventor	Sharad Saxena
Art Unit	2128
Examiner Name	Morella I Rosales Hanner
Attorney Docket Number	D5116-00002

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
H.D.		PELGROM et al., "Matching Properties of MOS Transistors." IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, SC-24, pp. 1433-1440, October 1989	
H.D.		SIDNEY SOCLOF, "Design and Applications of Analog Integrated Circuits." Prentice Hall, New Jersey, 1991.	
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H.D.		HANSON et al., "Analysis of Mixed-Signal Manufacturabiltiy with Statistical Technology CAD (TCAD), IEEE Transactions on Semiconductor Manufacturing, Vol. 9, No. 4, November 1996	

Examiner Signature	Hearog-del Ray	Date Considered	3/24/05

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